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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/034,458 | 12/28/2001 | Gyo Un Choi | CU-2797 VE | 9340 |

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| EXAMINER | |
|---|---|
| DIAZ, JOSE R | |
| **ART UNIT** | **PAPER NUMBER** |
| 2815 | |

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/034,458 | CHOI ET AL. | |
| | Examiner | Art Unit | |
| | José R Díaz | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

The drawings were received on January 23, 2004. These drawings are acceptable. However, the drawings are objected to under 37 CFR 1.83(a) because figure 3A fails to show the zigzag connection 30a connected to a first line D1 of the data even pad 17b as described on page 7, lines 15-17 of the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-3, 5-7, 9-11 are still rejected under 35 U.S.C. 102(a) as being anticipated by applicant's admitted prior art.

Regarding claims 1, applicant acknowledges a structure comprising: a TFT array unit (11) comprising a plurality of gate lines ($G_1 \ldots G_n$) and data lines ($D_1 \ldots D_n$) formed in a matrix shape (see figure 2), having TFT transistors at the intersection of the gate line

and the data line (see figure 2 and page 2, line 13); a data pad unit (17a, 17b) commonly connected to the plurality of data lines ($D_1 \ldots D_n$), receiving signals from driving the data lines (see fig. 2); and a wiring unit (consider the cone shaped wiring units extended between the pixel array (11) and the data pads (17a, 17b)) for testing defects of data line, connected between the data pad unit and the data line, testing disconnection and short of the data line (see fig 2 and page 2, lines 16-20).

Regarding claim 2, applicant acknowledges a structure comprising a first data pad unit (17a) commonly connected between odd data lines of the plurality of data lines, and a second data pad unit (17b) commonly connected between even data lines of the plurality data lines (see fig. 2).

Regarding claim 3, applicant acknowledges a structure comprising a first wiring unit (consider the wiring portions of the cone shaped wiring units extended between the pixel array (11) and the data pad (17a), and connected to the odd lines $D_1 \ldots D_{n+2}$) for testing defects of data line connected between the first data pad unit (17a) and the odd data line ($D_1$), and a second wiring unit (consider the wiring portions of the cone shaped wiring units extended between the pixel array (11) and the data pad (17b), and connected to the even lines $D_2 \ldots D_{n+2}$) for testing defects of data line connected between the second data pad unit (17b) and the even data line ($D_2$) (see fig. 2).

Regarding claim 5, applicant acknowledges a structure comprising: a TFT array unit (11) comprising a plurality of gate lines ($G_1 \ldots G_n$) and data lines ($D_1 \ldots D_n$) formed in a matrix shape (see figure 2), having TFT transistors at the intersection of the gate line and the data line (see figure 2 and page 2, line 13); a gate pad unit (15a, 15b)

commonly connected to the plurality of gate lines ($G_1 \ldots G_n$), receiving signals from driving the gate lines (see fig. 2); and a wiring unit (consider the cone shaped wiring units extended between the pixel array (11) and the gate pads (15a, 15b)) for testing defects of gate line, connected between the gate pad unit and the gate line, testing disconnection and short of the gate line (see fig 2 and page 2, lines 16-20).

Regarding claim 6, applicant acknowledges a structure comprising a first gate pad unit (15a) commonly connected between odd data lines of the plurality of data lines, and a second gate pad unit (15b) commonly connected between even data lines of the plurality data lines (see fig. 2).

Regarding claim 7, applicant acknowledges a structure comprising a first wiring unit (consider the wiring portions of the cone shaped wiring units extended between the pixel array (11) and the gate pad (15a), and connected to the odd lines $G_1 \ldots G_{n+2}$) for testing defects of gate line connected between the first gate pad unit (15a) and the odd gate line ($G_1$), and a second wiring unit (consider the wiring portions of the cone shaped wiring units extended between the pixel array (11) and the gate pad (15b), and connected to the even lines $G_2 \ldots G_{n+2}$) for testing defects of gate line connected between the second gate pad unit (15b) and the even data line ($G_2$) (see fig. 2).

Regarding claims 9-11, applicant acknowledges a structure comprising: a TFT array unit (11) comprising a plurality of gate lines ($G_1 \ldots G_n$) and data lines ($D_1 \ldots D_n$) formed in a matrix shape (see figure 2), having TFT transistors at the intersection of the gate line and the data line (see figure 2 and page 2, line 13); a common voltage pad unit (13) commonly connected to the common voltage line connected to each pixel (see

page 2, lines 12-14); and a wiring unit (consider the portion of the common voltage line close to the common voltage pad unit (13) as the wiring unit) connected between the common voltage line and the common voltage pad unit, testing disconnection and short of the common voltage line (see fig 2 and page 2, lines 12-20).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 4, 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Chung et al. (US Pat. No. 6,356,320 B1).

Regarding claims 4, 8 and 12, applicant's admitted prior art fails to teach a wiring unit having a zigzag shape. Chung et al. teaches that it is well known in the art to form a zigzag-wiring unit (85, G1, G2, G3, G4) (see Figs. 7-8, abstract and col. 4, lines 34-49).

Applicant's admitted prior art and Chung et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a zigzag-wiring unit. The motivation for doing so, as is taught by Chung et al., is eliminating stitching defects (abstract and col. 6, lines 10-17). Therefore, it would have been obvious to combine Chung et al. with Applicant's admitted prior art to obtain the invention of claims 4, 8 and 12.

***Response to Arguments***

Applicant's arguments filed January 23, 2004 have been fully considered but they are not persuasive.

With respect to Applicant's assertion that the prior art fails to teach the wiring unit, it is noted that during patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification" (see MPEP 2111). In the instant case, Applicant teaches in figures 3A and 3B of the specification that the wiring unit (30a, 30b) is merely a portion of the data line (D1 and/or D2). Thus, the upper cone shaped portion of the data lines (D1...Dn) shown in figure 2 of applicant's admitted prior art would read ~~over~~ on the claimed limitation.

***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on 9:00-5:00 Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD
4/29/04

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